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DESIGN, SIMULATION & COMPARISON OF NOVEL TG8T SRAM WITH TRADITIONAL SRAM DESIGN

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Abstract: **As technology is increasing rapidly, the usage of low power devices has become more usable. One among such is transmission gate 8T SRAM. Static random access memory has now a day's become an important feature in the VLSI chip design. SRAM has become a sustainable research due to its fast development for low power. Static random access memory plays most prominent role in the microprocessor world, but as the technology is scaling down in nanometers, leakage parameters and delay parameters are the most common problems for SRAM cell which is basically designed for very low power applications. This paper presents architecture of TG8T SRAM cell with an improved version of existing 8T SRAM cell, where all pass transistors are replaced with transmission gates.**

Keywords: *SRAM, Transmission Gate 8T, leakage power, delay .*

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I INTRODUCTION

The handy devices such as hand held mobile devices and special digital assistants are gaining more attractiveness as well as making changes in every phase of our daily life's. On chip cache represent a large portion of the chip and is expected to increase further in both moveable devices and high performance processors. Embedded memory access is more requisite in video applications, which results in momentous power consumption and confines the battery life. Owing to explosive growth of battery operated appliances, Power debauchery has become imperative reflection due to enlarged integration and operating speeds.

Low power design has become a catchphrase now-a-days and deceitful of low power devices has become a foremost constraint in the locale of simulation such as power constrained applications. Researchers have recommended that operating a circuit in sub threshold region can condense the power utilization to bare minimum achievable range. It is only possible when its sub-threshold voltage (Vth) is greater than supply voltage (VDD) applied..With scaling of MOSFET to sub nanometer technology data stability of SRAM bit cells is major problem.

Due to rapid increase in threshold voltage, 6T SRAM cannot operate in its efficient parameters in terms of Read &write operations[1], which results in the yield loss. Taking this drawbacks into consideration, we propose an transmission gate 8T SRAM cell (TG8T) where they can be operated both in terms of functionality and performance, and comparing their performance standards with standard 6T SRAM cell using synopsis tool and by using custom design model at 32nm technology.

The rest of the paper is organized as section II explains the architecture of 6T SRAM and its operation, section III describes about the single bit 8T SRAM schematic design and its operation. Section IV describes about the TG8T SRAM cell with its read and writes operations. The Final section describes the about the functionality and performance is estimated by read &write operations[2] along with power and delay analysis & comparison is made between these different design types.

II EXISTING 6TSRAM CELL

The architectural designs of 6T SRAM cell undergoes several changes with read and write operations. The Static Noise Margin (SNM) is less due to no proper separation between read &write operations. The amount of leakage power is marginally high when the technology is scaling to the higher levels. The read and write operations can be analyzed by the given 6TSRAM as shown below. When

b=1 and VDD=1,M3 turns ON and output of M3 is Q=1,makes M1.M4 ON state, where other transistors like M5 & M6 will turn OFF .therefore Qb becomes high and also bb is high, and vice versa when input b is low.

A. Architecture Of 6t SRAM

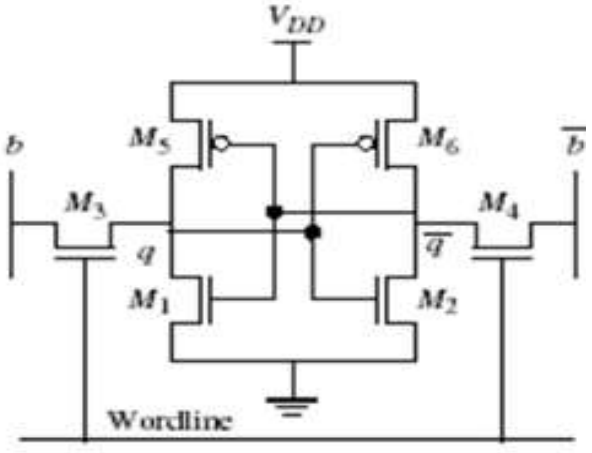

Figure 1.1 schematic of 6T SRAM cell

B Schematic diagram of 6t SRAM

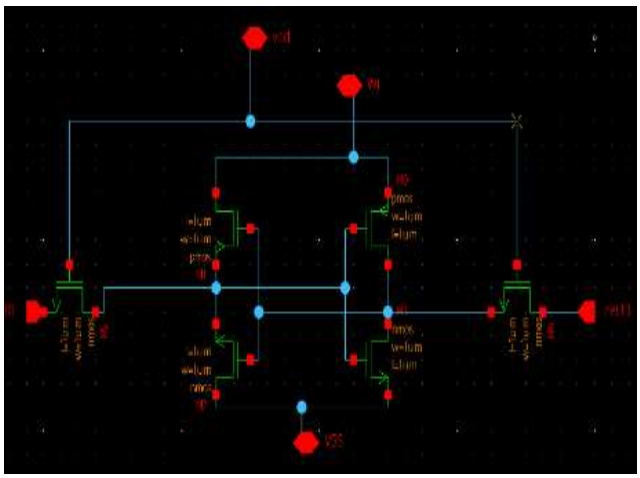

Figure 1.2 schematic of 6T SRAM cell

The Memory cell represents a CMOS static random memory. In this design each bit of SRAM is stored by forming a cross-coupled inverter circuit. This storage cell has two bi-stable states of operation i.e.; '1' and '0's. It is also treated as a bistable latch. SRAM uses 6 transistors as a cell, middle 4 transistor is connected as back to back cross-coupled connection. These four transistors are used to store the bit value either high or low; generally these transistors are made small to reduce the chip area and operate in weak inversion region. The first inverter circuit, has a low input value and it will generate high value to the second inverter, the second inverter produces, amplifies &stores the low data into it. Similarly high input value on the first inverter will generate low output amplifies & stores the data into it and fed back to a another inverter produces as low. The two lines between the inverter are connected to two n channel MOSFETs and are connected to bit line and bit line bar. In large SRAM models word line are acting like row and column lines. As long word lines are high and the inverters are feeding the inputs by themselves and store its current value [3] as showed Fig 1.1. In schematic of 6T, an hVth type of transistors is used in order to improve the stability of the circuit. The schematic model of 6T SRAM is designed in 32nm Technology is shown. The Standard sizes of length and widths are considered as to obtain proper characteristics along with power &delay.

C **Read &Write Operations**

SRAM is designed with the 6T cell which is having a high speed performance compared to Dynamic RAM, but the problem is high power consumption [2,3]. Number of researchers has made an attempt to improve stability, but it remains as it is, due to its static noise margin (SNM).The two transistors of n-type are acting like to serve the control of storage cells, the other 4 transistors are connected as an inverter & connected as feedback network. When the WL is high, the data is going to store into the bistable latch, which controls the access of M5 and M2. BL and BLB are used to transfer the data for read and write operations. Though it is not necessary to have both bit lines, it provides the exact noise margin between the read and write states. A sense amplifier is used to sense the logic differential voltage & make the value of the output stable at either 1 or 0 showed Fig 1.2.

The main advantage of 6T SRAM is less in static power but suffered from static noise margin[3]. It is obtained by mirroring the characteristics of inverter finding the best possible square between them and also called as butterfly curve. Though it has an importance in hold operation, it has a significant amount of importance in active mode. The value of the WL is high and bit lines are pre charged to the high value. The internal node of the cell is representing '0' gets pulled upwards through access transistors and driver transistor voltage, this degrades static noise margin [4].

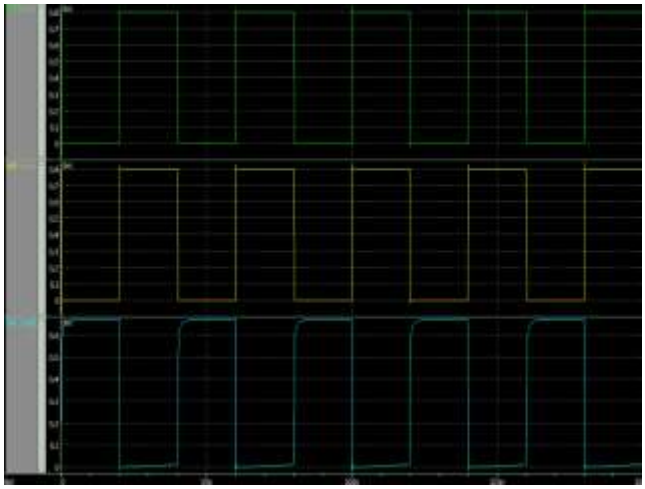

Figure 1.3 Simulation Result of SRAM

From Fig 1.3 The read & write characteristics of 6T are as shown above, when the word line is high, the value of BL is high, the output of BLB is low, performing read operation, and vice versa. This value separates the read and writes operation. The second inverter has the same input and produces high value at the output. This value will continue until completion of the write operation and the performs write operation. The value that is stored, will be read out WL is high and BL is high and BL BAR is low**.**

III 8-TRANSISTOR SINGLE BIT SRAM

The Main issue in the 6T congenital RAM is static noise margin, the read access can be potentially problematic. The two transistor M5and m6 drives one side of the logic low and other transistors logic makes high. The two other transistors M1 and M2 stores the reduced value of the cell. Especially the values changes in the logic with the variations in the supply voltage[5]. With reducing supply voltage the memory cell becomes susceptible to variations, especially threshold voltage changes due to random doping fluctuations and memory cell NMOS transistors (M1, M3). which makes the memory cell less reliable during this operation. The 8T cell address this issue by having separate transistors, one where data is written and hold (M1 to M6) and the other where data is read from (M7-M8) [6].

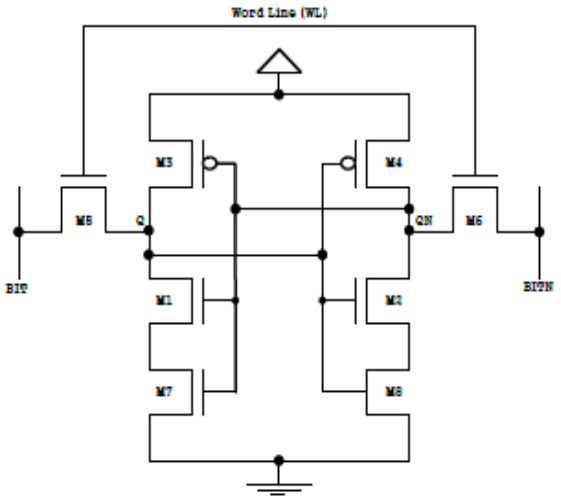

Figure. 1.4 8T SRAM design

The above Fig. 1.5 shows an implementation of SRAM using 8T modeling by additional two transistors are acting as pulled transistors [5], that Fig 1.5 Circuit diagram of 8T SRAM are added to the 6T SRAM cell circuit. The amount of static noise margin can be avoided in this case, by separating the read and write operation. In order to write the '1' into SRAM, WL is asserted as 1, and BL is made as high and BLB is low, the value of 0 is stored across 'BLB' and complement of B. After pre-charging Bit Line (BL=BLB=1), WL is pulling the one of the bit line low. But the stability of 8T SRAM data is increased, due to the single 8T SRAM, leakage current and data retention are greatly reduced among the major area of chip design today [6,7].

A. Design & Operation

The two cross-coupled inverters M1, M6 and M2, M4 [6] are connected to back and M5, M6 are access transistors. In order to achieve Static Power Reduction. The two additional NMOS transistors are used here are connected to the cross-coupled inverter circuit. The gate terminal of access transistors are connected to the word line and the bit line is connected to the terminal of the drain.To select the design cell, word lines are used and write, read operations are performed using bit lines. But internally cell holds the stored value of Q on its node & QB on the other node. These complementary BL's are used to perform read & write operation. From the below diagram, we can consider that the circuit is symmetric, and therefore M1=M2, M4=M6, M6=M6, and M7=M8 as showed Fig 1.5

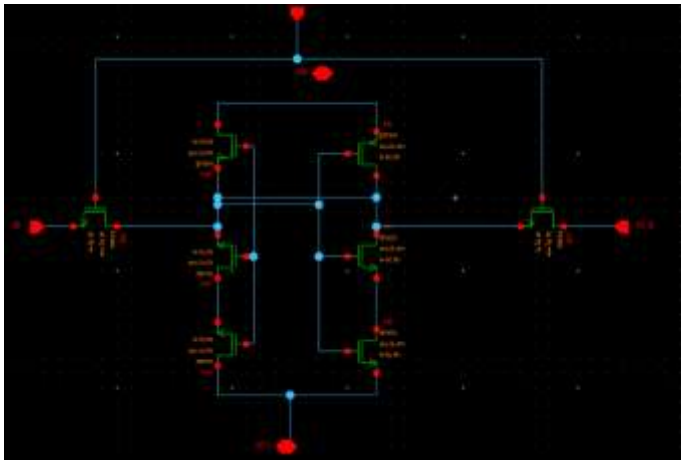

Figure 1.5 Schematic of 8T SRAM

In the schematics, we use hvt type of transistors are used to reduce the Static Power, and this schematic implemented 32nm are indicated as below Fig 6.4.

B. Read & write operation

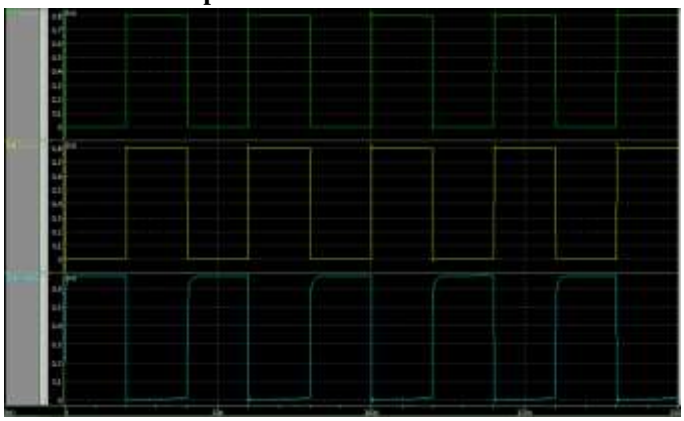

Figure 1.6 Simulation Result of of 8T SRAM

During a WRITE operation, the BL is pulled to VSS (writing “0” and BL bar is kept at VDD. the source of the left inverter is reduced (BL pulled to VSS). The trip point of inv becomes lower because of the reduced strength of PMOS

transistor of inv. The source voltage of PMOS transistor of right inv is at VDD enabling a faster pull up for the complementary node.

III NOVEL DESIGN OF 8T SRAM USING TRANSMISSION GATE

The continuous calling down of bulk CMOS creates major issues due to its base arterial. The primary obstacles to the Scaling of bulk CMOS to 32nmgatelengths includes short channel effects ,Sub-threshold leakage, gate-dielectric leakage and device to device variations. Due to sudden increase in threshold voltage i.e. V to oscillation produced by overall and general process variations occur in ultra-short-channel devices, 6T SRAM cell and their modifications cannot be operated at advance scaling of supply voltages without functional and parametric failure causes yield loss. The design of standard 6T SRAM cell undergoes a lot of problem on write delay [8].The design of Low power 6T SRAM cell could decrease the write power and access delay [8] but could not improve their stability. In deep submicron ranges, none of the earlier works has studied about the improvement of variability in SRAM cell at the schematic level. Therefore, we design a vigorous and variation accepting SRAM cell design technique capable of gripping Vt shift due to random doping fluctuation(RDF), and variation in further device and their process parameters (such as length, width, sub-wavelength-lithography, oxide thickness, etching, and annealing) and still be able to perform expected functions need to be investigated. To fulfill this drawback we propose a transmission gate 8T SRAM cell (TG8T) and compare their performance with standard 6T,8T SRAM cell at synopsys circuit designer tool at 32nm technology.

A. *Architecture of TG8T SRAM cell*

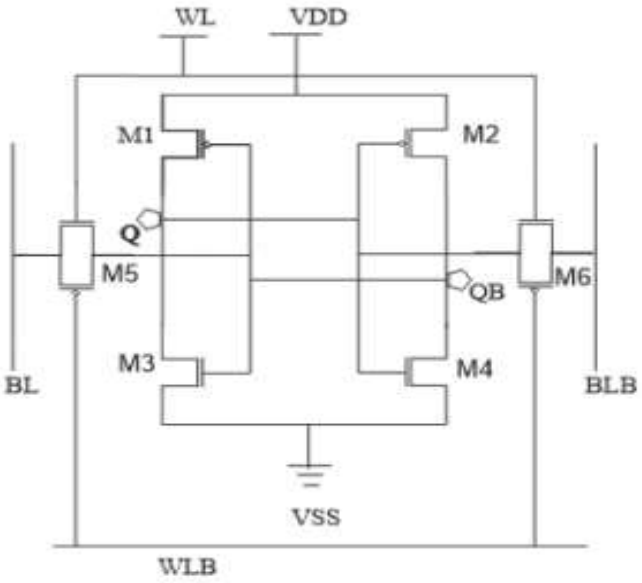

Figure 1.7 TG8T SRAM cell.

B. *Schematic model* using transmission gate

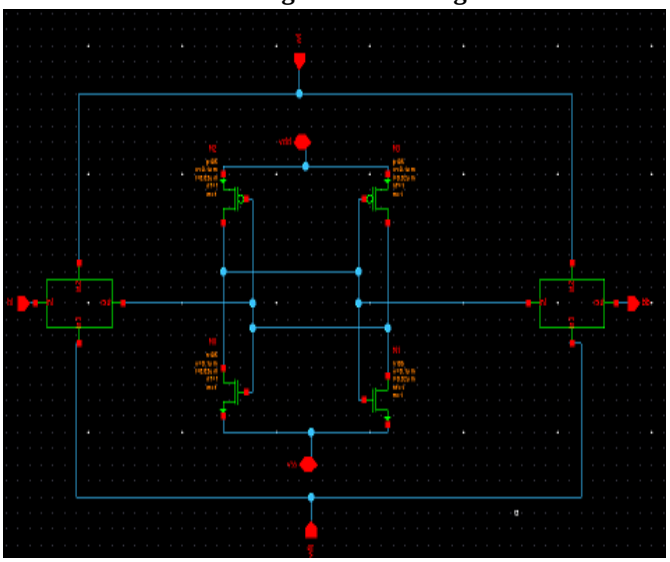

Figure 1.8 schematic representation of TG8T SRAM

C. *Working of TG8T SRAM cell.*

The working of TG8T SRAM cell consist of two operation i.e. write and read operation. When we performing a write operation ,both the bit lines are at opposite voltages which represent if bit line BL is at high then BLB is at low and vice versa (BL=1 and BLB =0 or BL =0 and BLB =1) [8,9]. When WL becomes high and also WLB =0 which enables NMOS and PMOS transistors M5 and M6 then data writes on the output nodes Q and QB of back to back connected inverter. When we perform the read operation which is just opposite to the write operation, both the bit lines are at high voltages also behave as an output and WL is raised to high and WLB at 0. Since one of the output nodes (Q and QB) is at low then one of pre-charged bit lines start discharging and at that instant data is going to be read

D. *Power analysis:*

Static Power

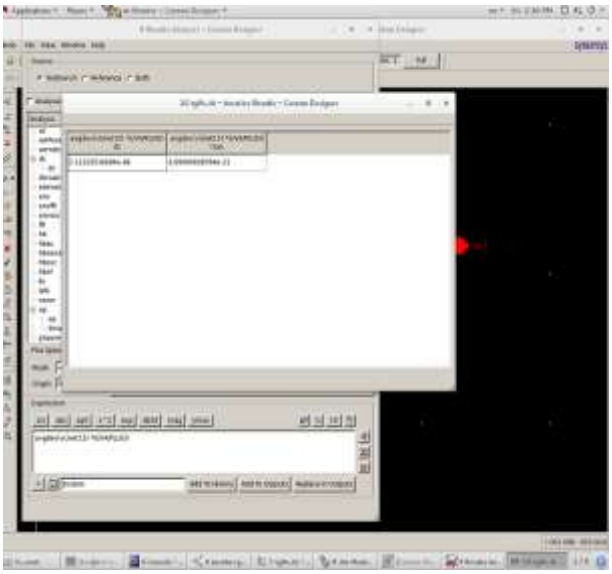

Figure 1.9 static power analysis 6.69

Dynamic Power

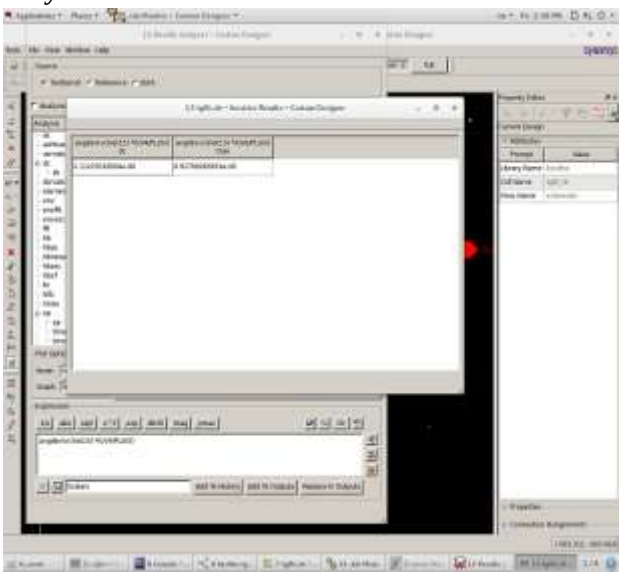

Figure 1.10 Dynamic power

E. DEALY ANALYSIS

Rise time analysis

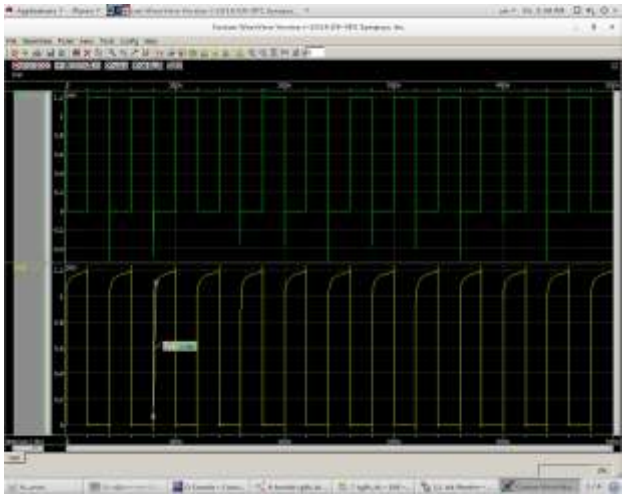

Figure 1.11 Rise time Analysis

Fall time analysis

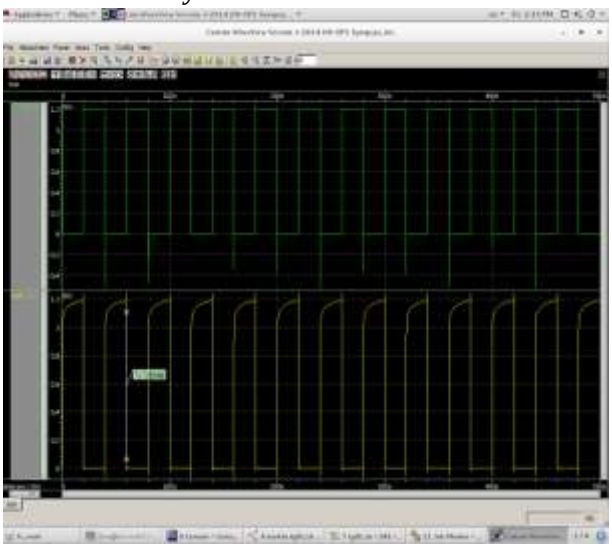

Figure 1.12 fall time Analysis

IV COMPARISON & ANALYSIS

Table 1.0 comparative analysis

Parameters	6T SRAM	8T SRAM	TG8T SRAM
Static Power in nw	1.60E-10	3.48E-11	6.69E-21
Dynamic Power in nw	4.70E-19	2.31E-20	3.70E-27
Total Delay in in ps	8.90E-11	7.41E-11	2.32E-21

Comparative analysis is dine with respect to power & delay. The static & dynamic power is gradually decreased in TG8T SRAM and in the other way the amount of delay also reduced. Therefore the TG8TSRAM is the replacement for low power and high frequency like bio medical applications EEG, ECG, Pacemakers, where they need to run years together inside the human body with low power consumption.

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