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SIMULATION AND ANALYSIS OF TEMPERATURE EFFECT ON 7 nm n-MOSFET

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Abstract: In this paper, a detailed study has been performed to investigate the temperature effect of drain current, threshold, transconductance and sub-threshold leakage current of 7nm MOSFET. To execute this study, simulations were carried out using HSPICE simulator. Investigation of temperature effect ranging from -60 to 20˚C was carried out throughout the study. The performance of MOSFET was estimated through drain current, threshold voltage, and transconductance and sub-threshold leakage current. Linear decrease in drain current and threshold voltage with increase in temperature was observed. Lowering the temperature, the current of MOSFET raises because of mobility of electrons & holes increased. HSPICE is friendly software which helps to successful process of implementation and data extraction.

Keywords: *BISM, Threshold Voltage, Sub-threshold leakage current, Transconductance and HSPICE.*

I INTRODUCTION

MOSFET technology has been used in different digital and analog electronics applications. It has become a backbone of semiconductor industries of modern electronics [1].Carrier mobility of NMOS and PMOS are 1400 cm^2/Vs and 450cm^2/Vs respectively [2].Carrier mobility of NMOS is higher than PMOS, therefore NMOS is used for high speed since as compared to PMOS. While as compared the cross sectional area NMOS is smaller than PMOS.As junction area is smaller and drain current is higher than PMOS, so the NMOS perform faster than PMOS [3].MOS high performance technology can be deal with power dissipation for complex integrated circuit such as microprocessor. But for low operating power technology with high performance applications, then we have to reduce the power consumption of operating circuit. To reduce the power consumption by decrementing the supply voltage as low as possible [4].

To deal with the power consumption with higher performance, scaling of MOSFET technology is essential [5]. As scaling down the MOS technology continually improving the performance as more and more devices packed in smaller area of chip. So scaling is attractive due to electrical compatibility with existing circuit. So, when during a scaling, trade off among the performance and compatibility of existing technology, reliability, complexity and device performance, scaling technology has been providing a very essential technology for microelectronics.

At the early stage in 1971, 10μm channel length MOSFET has been used, then after 1997, 250nm MOSFET have been served to electronics. As speed improvement is 20% and area decremented by 30% per year [7], though from 250 nm to 7 nm technologies, there are largest change in performance, area of circuits, cost and power per function. As finFET technology has been introduced in nanotechnology, but there is a poor short channel control [8].

MOSFET technologies have superior scalability, improved transport properties and CMOS compatibility. The schematic of nMOSFET is shown in Figure1

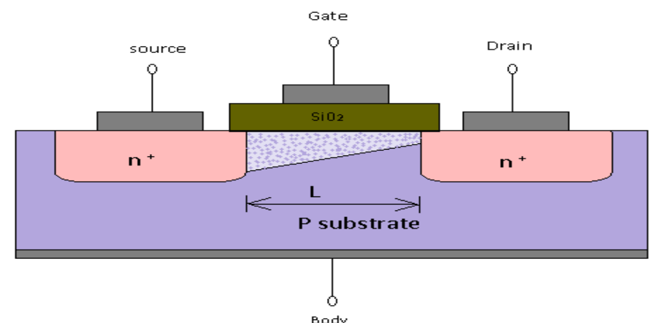

Figure 1 Model structure of N type MOSFET

While doing a scaling, density of circuit is increased due to that raise in temperature. Hence, it is very important to understand the effect of temperature on device while scaling down technology [9].For low power consumption with high density packages on chip, we have to reduce a supply voltage [10], but are some limitations in scaling down a voltage. However scaling technology served a crucial technique to reduce a supply voltage with high package density. Drain current is mainly dependent on supply voltage, however scaling down the technology it is very urge to find out effect of temperature on drain current [11]. From the literature, we can say that drain current is affected by temperature with scaling down technology [12].

To reinforce the performance of MOSFET without miniaturization, we can use a low temperature technique [13]. This is useful for no. of application like aerospace application, satellite applications, high-sensitivity cooled sensor, terrestrial space mission and low noise receiver [14]. These are applications for a different low temperature to study the performance of device. Due to reduction in temperature there are some parameters which are affected like threshold voltage, drain current, transconductance and sub-threshold leakage current [15] - [19].

Here we have used BSIM4 model of 7nm MOSFET for simulation. To study effect of temperature on 7nm MOSFET, PTM file of 7nm MOSFET is used to simulate using a HSPICE 2008.3 simulator. This was gives an idea about the performance of 7nm device over low temperature. Study the temperature dependent parameters is very important while lowering the temperature. Drain current with temperature dependent is change by the variation in the threshold voltage, mobility and saturation velocity [14]. Drain current is mainly dependent on supply voltage, thereby the drain current is less dependent on temperature while scaling [15].There is excess scattering as temperature increases which causes the higher in effective resistance [16]. Hence drain current decrease with temperature increases.

It is very crucial to study the effect of low temperature on performance of 7 nm MOSFET device. Here from the equation we can say effect of low temperature ranging from -60℃ to 20℃ on carrier channel, mobility is high, therefore it directly affects to the drain current. Mobility raised at lowering temperature due to less scattering. Drain current of MOSFET is derived using some basic [17].

$$I_d = \mu C_{ox} \frac{W(V_{gs} - V_{ds})^2}{2L} \quad (1)$$

The above equation can be used to represent the MOSFET model. In this equation, C_{OX} is the capacitance of the oxide layer. μ is the charge-carrier effective mobility, L is channel length.

While studying of temperature dependence characteristics of MOSFET, The threshold voltage is very important parameter. Drain current of MOSFET is proportional to threshold voltage and gate voltage therefore any small variation causes a larger change in drain current (I_d). Thus the temperature dependent study of threshold voltage is very important and many parameters are associated to the threshold voltage while studying the temperature dependent characteristics MOSFET [18]-[19].

$$\frac{\delta V_{th}}{\delta T} = \frac{\delta \Phi_F}{\delta T}\left[\alpha \sqrt{\frac{q \epsilon_{si} N_{eff}}{\Phi_F {C_{ox}}^2}} + 2 + \frac{q D_{it}}{C_{ox}}\right] \quad (2)$$

Where Є_si and q are the silicon permittivity and electron charge; α = 1 for partially depleted devices and α= 0 for fully depleted transistors. Eq. (2) increases when the temperature decreases [20].

Sub threshold leakage current is also an important temperature dependent parameter. When transistor is in OFF mode, there is current flow in between source to drain current called sub-threshold leakage current. The Sub-Threshold is term from gate voltage V_{gs} is smaller than threshold voltage. It is very important to find out the power dissipation of device [21]-[22].An accurate estimation of the sub-threshold behavior by means of physical modeling is important for the device and circuit [23]. The following equation shows the sub-threshold leakage current of MOSFET which is denoted by I_{Sub} [24].

$$I_{Sub} = \frac{\mu W_{eff} C_{ox}}{L_{eff}} {V_T}^2 e^{(|V_{GS}|-|V_t|)/\eta V_T}\left(1 - e^{-|V_{DS}|/V_T}\right) \quad (3)$$

Where W_{eff} is Effective transistor width and L_{eff} is Effective channel length, η is Sub-threshold swing coefficient and V_T is Thermal voltage.

Analysis of transconductance G_m in linear and saturation low temperatures using analytical expressions for gm derived by using simple square law MOSFET current model [25]-[27].

$$G_m = \frac{\beta(T) V_{ds}}{2} \quad (4)$$

II.RESULT AND DISCUSSIONS

We pay particular attention to the low temperature and electric field. Figure 2 (a) and (b) shows the current-voltage characteristics of MOSFET at different temperature. To verify the model of MOSFET, the I-V characteristics of MOSFET with different temperature has shown. Temperature effect on current-voltage gives an idea about the performance of device while variation in temperature. Figure 2 (a) and (b) shows simulated drain current of MOSFET with channel length of 7 nm measure at different temperature. A simulated result of I-V Characteristics at different temperature explained temperature dependent shift in drain current. While

keeping the supply voltage 0.7V, Figure 2 (a) shows the comparison of simulation of transfer I-V characteristics at different temperature. We performed for n-MOSFET at fixed V_{ds}=0.7V.In Figure 2 (b) I-V curve shows the output characteristics of same MOSFET at different temperature with keeping V_{gs}=0.7V.

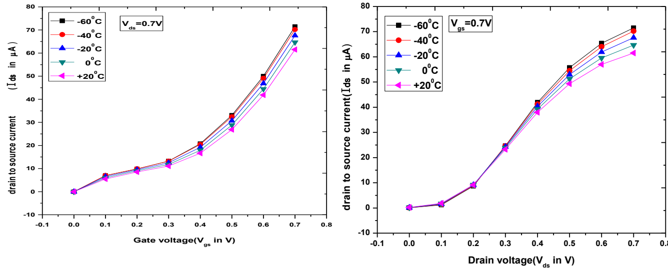

Figure 2 (a) Transfer characteristics with different temperature (b) Output characteristics at different temperature.

The simulated temperature dependent data obtained for low temperature range -60˚C to 20˚C.Here temperature increasing the drain current falls with linearly in all cases. Typically Fig.3 (a) shows drain current verses temperature with fixed V_{gs}= V_{ds}= 0.7 V. The negative temperature range -60˚C to 20˚C the drain current changes from 71.5 µA to 61.5 µA respectively. From this graph, it is clear that increasing temperature cause a decrease in mobility [16]. If this decreases mobility is almost dependent of drain current. Drain current decreases constantly for various fixed values of supply voltage as temperature increases.

Threshold voltage is important parameter in study of temperature dependence of MOSFET characteristics. Change in V_{th} with temperature are shown and compared with measured data as shown in Fig.3 (b).

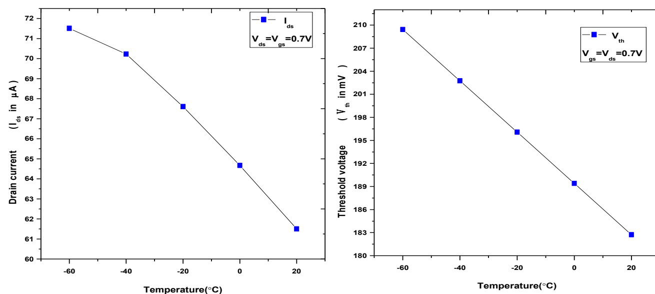

Figure 3: (a) Drain current variation with temperature (b) Threshold voltage variation with temperature with V_{gs}=V_{ds}=0.7V

As the temperature reduced the threshold voltage increased because when temperature decreases carriers in channel become freeze. So that higher gate voltage should be provided to invert the channel [19].MOSFET has a V_{th}= 182mV at room temperature and V_{th}=209mV at -60˚C.There is large variation of threshold voltage cause in drain current of MOSFET. It has been observed that most of current change about 11% on an average is due to a threshold voltage [14].Drain and source resistance change monotonously with temperature.

Use A transconductance at gate biases close to threshold voltage will drops gradually with temperature due to mobility degradation with temperature [26]. Characteristics for NMOS of $^{W}/_{L}$ = $^{14}/_{7}$ standard CMOS process at various temperatures are shown in Fig. 4 (a) and (b).In this, a V_{gs}=0.3V identified maximum variation in transcoductance. As temperature increases, G_m gradually decreases due to mobility reduction with temperature while threshold voltage reduction with temperature has negligible effect on G_m in the linear region as indicated by equation (4).

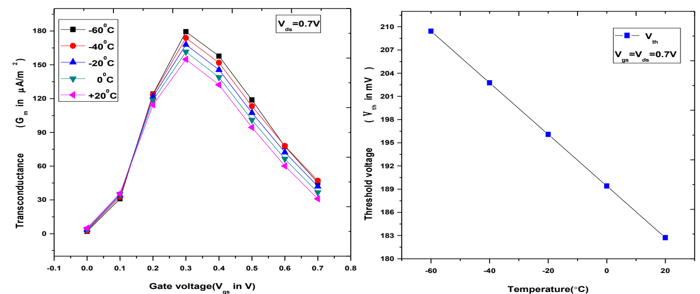

Figure 4 (a) Transconductance variation with gate voltage (V_{gs}) at different temperature at V_{ds}= 0.7V (b) Transconductance (Gm) variation with temperature

The Effect of temperature on sub-threshold leakage current is essential in digital VLSI circuits. Simulation of Sub-threshold leakage current with different temperature is shown in Fig 5.In offset state of mode the sub-threshold leakage increased linearly with increased in temperature and voltage [22]. Fig 5. Shows the variation in sub-threshold leakage current in various temperature ranging from -60ºC to 20ºC with V_{ds}=0.7V.

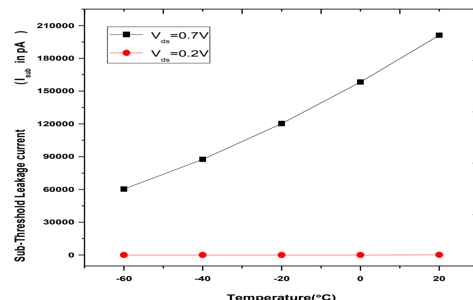

Figure 5: Sub-threshold leakage current variation with temperature at V_{ds}=0.2V and V_{ds}=0.7V

It can clearly be seen that for different V_{ds} varying from 0.7 V to 0.2V a significant reduction in sub-threshold leakage current. At V_{ds}, it rises exponentially with temperature [22]. At temperature (-60°C) and V_{ds}= 0.7 V, I_{leak} is $62.491E^{-9}$ A, while at temperature (20°C) and V_{ds}=0.7V it goes up to $204.17E^{-9}$ A i.e 69% change. At temperature (-60°C) and V_{ds}=0.2V, I_{leak} is $147.58E^{-12}$ A while at temperature (20°C) and V_{ds}=0.2V it goes to $13.61E^{-12}$ A i.e 91% change. So it is conclude that this change is very high. Therefore as Temperature change, the effect become prominent on leakage current.

III CONCLUSION

The work is done with focus of parameters of 7nm n-MOSFETs, which can be useful in low temperature applications. Devices showed an increasing due to the increasing the mobility of charge carriers of channel as a reduction in temperature. As the threshold voltage and mobility increased at lower temperature so we can say that drain current improved at lower temperature. It clear from graphs the threshold voltage, transcoductance and sub-threshold leakage current depending upon temperature. The graph of transconductance characteristics is an image of the variation of electron concentration in the channel with temperature. Transconductance is increase in linear region but decreases in saturation region.

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